STATISTICS, OPTIMIZATION AND INFORMATION COMPUTING
Stat., Optim. Inf. Comput., Vol. **10**, February 2022, pp 135–146.
Published online in International Academic Press (www.IAPress.org)

Whale Inspired Optimization Algorithm for Optimal Design of Low Voltage Amplifier

Abdelaziz Lberni [1,*], Malika Alami Marktani [2], Abdelaziz Ahaitouf [3], Ali Ahaitouf [1]

[1] *SIGER Laboratory, Faculty of Sciences and Technology, University of Sidi Mohamed Ben Abdellah, P.O. Box 2202, Fez, Morocco*
[2] *SIGER Laboratory, National School of Applied Sciences, University of Sidi Mohamed Ben Abdellah, P.O. Box 72, Fez, Morocco*
[3] *SI Laboratory, Polydisciplinary Faculty of Taza, University of Sidi Mohamed Ben Abdellah, P.O. Box. 1223, Taza-Gare, Morocco*

Abstract This paper discusses the application of a new nature-inspired optimization algorithm, called Whale Optimization Algorithm (WOA), to the resolution and optimization of single- and multi-objective problems in microelectronic design field. The performances of WOA are tested on one of the more interesting analog integrated circuits (ICs), for low supply voltage applications, the low-voltage amplifier (LVA). After identifying and determining the constraints of the LVA circuit, WOA is used to optimize MOS transistors sizes. This allows the best gain, the largest bandwidth and the highest slew rate. These main characteristics are optimized in two ways. In the first step, each function is optimized on its own, keeping the others fixed. In the second, the three characteristics are combined, with equal weights, to form a single main objective function. WOA is coded in MATLAB and the obtained results are confirmed by Cadence Virtuoso simulations in CMOS $0.18\mu\mathrm{m}$ technology. The simulation results are $88.8\mathrm{dB}$ ($88.73\mathrm{dB}$), $23.92\mathrm{V}/\mu\mathrm{s}$ ($20.52\mathrm{V}/\mu\mathrm{s}$) and $24.6\mathrm{MHz}$ ($25.5\mathrm{MHz}$) for DC gain, slew rate and gain bandwidth in the single (multi)-objective experiment, respectively, justifying that WOA is an effective method for the design of the above mentioned circuit.

Keywords Low voltage amplifier, Analog IC Design, Equation-based method, Particle Swarm Optimization, Ant Colony Optimization, Whale Inspired Optimization Algorithm

DOI: 10.19139/soic-2310-5070-1204

1. Introduction

In the past years, the significant growth of consumer electronics devices triggered a major increase in micro- and nano-electronics activities, allowing the IC market to grow from almost $10 billion in 1980 to more than $400 billion in 2020 (World Semiconductor Trade Statistics) [1]. Due to the continuous progress in VLSI technologies, engineers are able to integrate in a single chip, the whole necessary electronic compounds for a System On Chip (SOC). Generally, integrated electronic circuits are composed of digital and analog parts. Analog circuits form the dominant block of electronic systems serving as an interface between digital parts and real signals [2]. These circuits are formed of hundreds of transistors and their importance cannot be neglected as their size imposes major constraints on their design, overall cost and performance [3]. If the digital IC design is an automatic task, the analog IC design remains a time-consuming, iterative and complex process. Achieving analog circuit design within strict time to market constraints is a real challenge. This is because of the demand for devices with lower production costs, better efficiency and integration costs, and lower design costs. New analog IC optimization and design methods should then be introduced to ensure optimal performance of the solutions regarding the design specifications. For simple specifications, circuits with one to two functions and few parameters, can be designed

*Correspondence to: Abdelaziz Lberni (Email: abdelaziz.lberni@usmba.ac.ma.). SIGER Laboratory, Faculty of Sciences and Technology, University of Sidi Mohamed Ben Abdellah, P.O. Box 2202, Fez, Morocco.

ISSN 2310-5070 (online) ISSN 2311-004X (print)

using the knowledge of designers [4]. However, for more complex circuits with a large number of transistors and many functions and constraints, one of the most challenging tasks for designers is to choose the optimal design respecting the constraints. The accomplishment of this difficult task is possible because designers are supported by computer-aided design tools assisting in the overall design process. Therefore, efficient simulation-based optimization techniques [5–11] or models-based techniques [12–18] are important for the optimal design of high-performance analog circuits. Metaheuristic optimization algorithms are recommended in such a case to generate good solutions in a reasonable time because they: 1) rely on quite simple concepts and are easy to implement; 2) can bypass local optima; 3) can be used for a wide range of problems in different disciplines [19]. Several metaheuristics have been suggested for the optimization of analog circuits, namely, particle swarm optimization (PSO) [20], butterfly optimization algorithm (BOA) [12], ant colony optimization (ACO) [21], genetic algorithm (GA) [22], simulated annealing (SA) [23], grey wolf optimization (GWO) [24], etc., These algorithms have proved to be useful and interesting in this field and their variety clearly shows that the debate remains open and that new methods are welcome to enrich this field of investigation. In this paper, we present an adaptation of the WOA algorithm for the analog integrated circuit design. The two-stage amplifier for low supply voltage applications is used as a complex circuit for testing the performance of the proposed optimization algorithm. The conception is performed in the CMOS $0.18\mu m$ technology parameters. The optimization results obtained by the WOA were evaluated and confirmed by the Cadence Virtuoso tool in the framework of the same technology. Simulation results show that the WOA algorithm works well and reaches its optimal results, corresponding to the required specifications for the circuit, much faster than other methods with even improved characteristics.

This paper is organized as follows: In section 2 the proposed algorithm details and its evaluation are presented. Section 3 presents the optimization of the analog circuit and the simulation results using Cadence Virtuoso. Section 4 shows simulation results and discussion. Finally, section 5 concludes the paper.

2. Whale Optimization Algorithm

The whale optimization algorithm is one of the recent nature-inspired meta-heuristic algorithms. Proposed by Mirjalili et al. in 2016 [19], WOA is a population-based approach. It is inspired by the special hunting technique of humpback whales. This technique is called the bubble-net feeding. In this feeding method, humpback whales swim around the prey and form a distinctive air bubbles around a circle or 9-shaped path. For more details about the bubble net feeding and hunting methods, see reference [19].

2.1. Encircling prey

Humpback whales are able to recognize the position of prey and encircle them. As the optimal design position in the search space is not known a priori, the WOA approach assumes that the target prey is the best current solution. Then, all other search agents try to improve their positions in relation to the best search agent. This procedure is expressed by [19] :

$$\vec{X}(t+1) = \vec{X}^*(t) - A.\vec{D} \tag{1}$$

$$\vec{D} = \mid C.\vec{X}^*(t) - \vec{X}(t) \mid \tag{2}$$

Where

$$A = 2a.r - a \tag{3}$$

$$C = 2r \tag{4}$$

C and A are coefficient vectors, $\vec{X}$ and $\vec{X}^*$ are respectively the actual and the best position vector obtained so far. $\vec{X}^*$ is updated at each iteration t if a new better solution is found. r is a random vector in [0,1] and a is linearly decreased from 2 to 0 over the iterations.

2.2. Bubble-net feeding method

The bubble-net feeding of humpback whales (exploitation phase) can be modeled by two approaches:

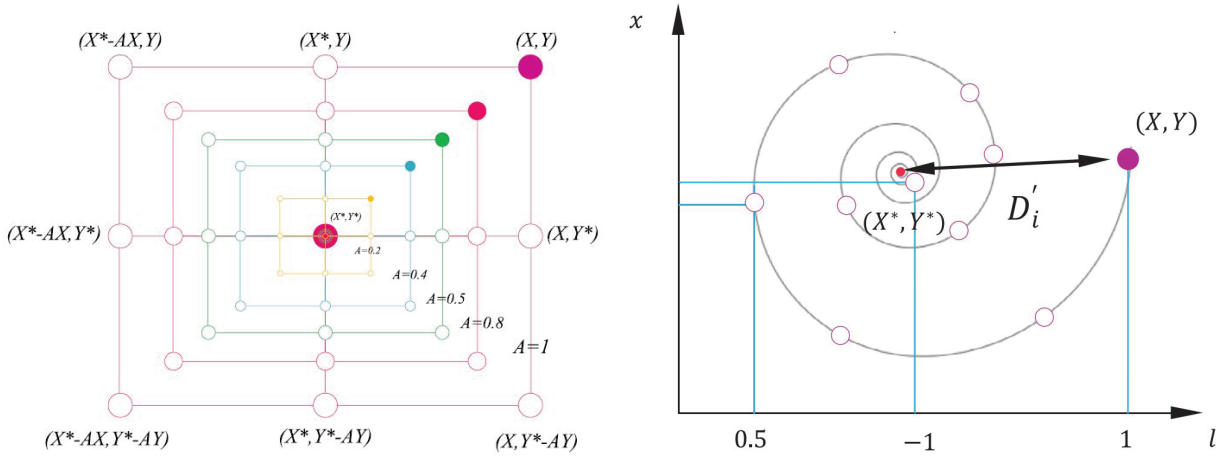
2.2.1. Shrinking encircling prey This behavior can be obtained by decreasing a in Eq. 3. This means that A is a random value in $[-a, a]$. Using random values for A in $[-1, 1]$, the new position can be set anywhere between the original agent and the current best agent positions. Figure 1a shows the possible positions from (X, Y) to (X^*, Y^*) which can be achieved by $0 \leq \mathrm{A} \leq 1$ in a $2D$ space.

2.2.2. Spiral updating position As can be seen in Figure 1b, this method first calculates the distance $\vec{D}^{'}$ between the located whale at (X,Y) and located prey at (X^*, Y^*). A mathematical spiral equation to update the position of humpback whale to prey is created to mimic the helix-shaped movement of whales is given by:

$$\vec{X}(t+1) = \vec{D}^{'} e^{bl} (\cos 2\pi l) + \vec{X}^*(t) \tag{5}$$

$$\vec{D}^{'} = \mid \vec{X}^*(t) - \vec{X}(t) \mid \tag{6}$$

Where $\vec{D}^{'}$ is the distance between the i^{th} whale to the prey, b is constant equal to 1 and l is random number in $[-1, 1]$.



(a) Shrinking encircling mechanism

(b) Spiral updating position

Figure 1. Bubble-net feeding methods of WOA [19].

Humpback whales all swim simultaneously around the prey within a shrinking circle and along spiral path. To model this behavior, we assume that there is a 50% probability (p) of choosing between the spiral model or the shrinking circling mechanism to update the position of the whales during optimization. Considering p as a random probability in the interval $[0, 1]$, we consider the smallest probability for the shrinking swim and the highest for the spiral trajectory as indicated by Eq. (7):

$$\vec{X}(t+1) = \begin{cases} \vec{X}^*(t) - A.\vec{D} & \text{if } p < 0.5 \\ \vec{D}^{'}.e^{bl}.(\cos 2\pi l) + \vec{X}^*(t) & \text{if } p \geq 0.5 \end{cases} \tag{7}$$

2.3. Search for prey

The same method based on the variation of A can be used to search for prey. Indeed, humpback whales randomly search depending on the position of others. Therefore, to force the search agent to move far away from a reference whale, we use A with random values less than -1 or greater than 1. Unlike the exploitation phase, the position of a search agent in this phase is updated by a randomly selected search agent instead of the best search agent found so far. This mechanism with $\mid A \mid > 1$ allow the WOA algorithm to perform a global search. The mathematical model is given by :

$$\vec{D} = \mid \vec{X}_{rand} - \vec{X} \mid \tag{8}$$

$$\vec{X}(t+1) = \vec{X}_{rand} - A.\vec{D} \tag{9}$$

Where $\vec{X}_{rand}$ is randomly chosen from the current population of whales.

The WOA approach begins with a population of random solutions, then at each iteration, the search agents update their positions either on the best solution obtained to date, or on a research agent selected at random. The parameter a is linearly decreased from 2 to 0 over iterations to ensure exploration and exploitation, respectively. When $\mid A \mid < 1$, the best solution is chosen, while a random search agent is selected when $\mid A \mid > 1$ to update the position of search agents. Finally, WOA stops when the stop criteria are met. The proposed algorithm is given in Figure 2.

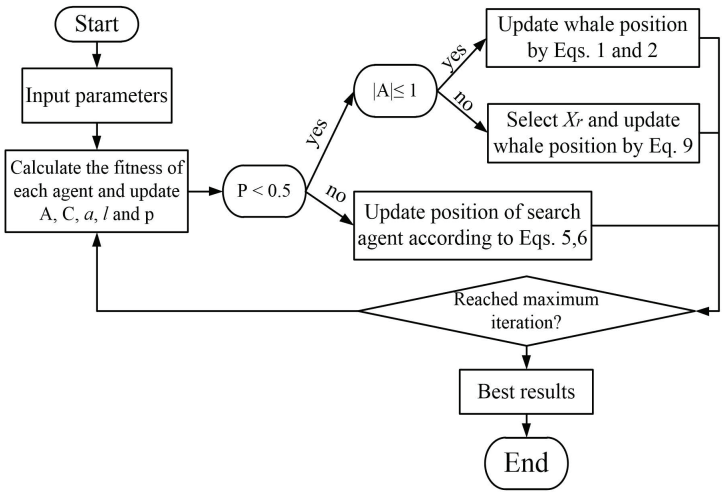


Figure 2. Flowchart of proposed WOA algorithm.

2.4. Evaluation of the used algorithms

The robustness of the proposed and used, for comparison algorithms, is tested by using mathematical classical test functions. Table 1 present the used functions, the variable limits and theoretical results and experimental minimums achieved by the algorithms for a population of 100 and 1000 iterations. The experimental results show that all algorithms achieve good results, we can also notice that WOA achieves a global minimum of each function and can be successfully used for optimization problems.

Table 1. Test functions and their variable limits as well as their theoretical and experimental minimums determined by the algorithms.

Functions	Ranges	$f_{\min}$	WOA	PSO	ACO
$f_1(\mathrm{x})=\sum_{i=1}^{Dim} x_i$	$[-100, 100]$	0	2.78E-32	1.20E-19	5.10E-07
$f_2(x)=\sum_{i=1}^{Dim}(\lvert x_i+0.5\rvert)^2$	$[-100, 100]$	0	2.85E-08	3.12E-06	1.27E-08
$f_3(x,y)=\sum_{i=1}^{Dim} ix_i^4+rand(0,1)$	$[-1.28, 1.28]$	0	6.36E-06	1.68E-04	1.01E-03
$f_4(x)=\sum_{i=1}^{Dim}(x_i^2-10\cos(2\pi x_i)+10)$	$[-5.12, 5.12]$	0	0.00E-00	0.00E-00	0.00E-00
$f_5(\mathrm{x})=\frac{1}{4000}\sum_{i=1}^{Dim} x_i^2+\prod_{i=1}^{Dim} cos(\frac{x_i}{\sqrt{i}})+1$	$[-600, 600]$	0	0.00E-00	0.00E-00	3.20E-12

3. Application of the WOA for the optimal design of the LV Amplifier

3.1. The low voltage two stage amplifier

Figure 3 shows the schematic diagram of the low-voltage two stage CMOS operational amplifier under study. It is formed from a simple n-channel differential input stage with current source loads (M3-M4), allowing the largest possible Input Common Mode Range (ICMR) without cascode or parallel input stages. M6 and M7 are biased so that the voltage across the sources and drains of the M3 and M4 corresponds to the saturation voltage $V_{SD}(sat)$. The output current signals of the differential stage are folded across M6 and M7 transistors and converted to the output stage with M8 and M9. C_C and C_L are respectively the compensation capacity and the load capacity. The main advantages of this amplifier topology in comparison to the traditional two-stage amplifiers are: high gain, lower supply voltage, balanced input differential stage loads [25].

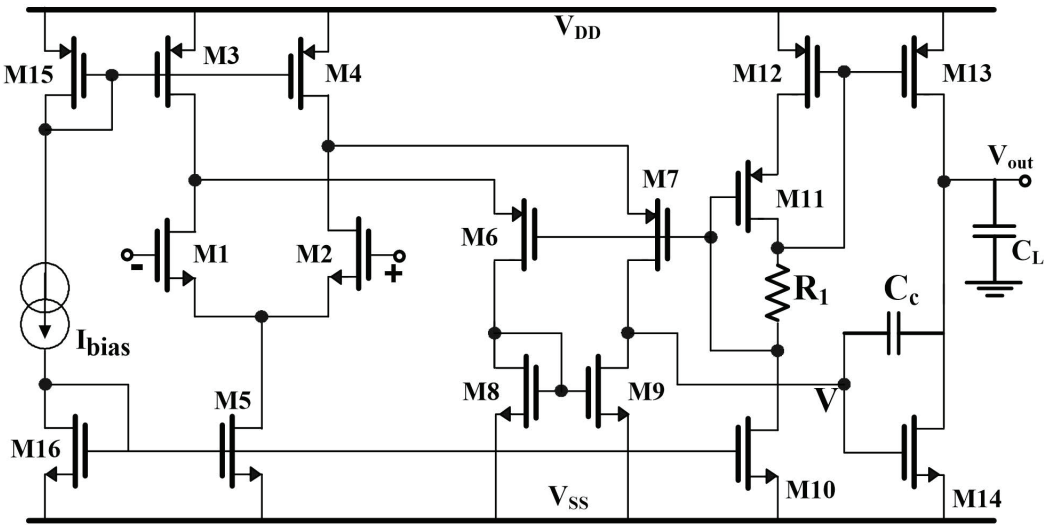


Figure 3. Low voltage two stage amplifier

The targeted optimal characteristics are: the DC gain, the bandwidth and the slew rate:

3.1.1. Voltage gain The open loop voltage gain is the product of the first and second stage gains :

$$A_v = \left(\frac{g_{m1}}{g_{ds7} + g_{ds9}}\right) \times \left(\frac{g_{m14}}{g_{ds13} + g_{ds14}}\right) \tag{10}$$

where g_{mi}, g_{dsi} are respectively the gate trans-conductance and the output conductance of i^{th} transistor.

3.1.2. Slew Rate The slew rate SR is given by:

$$SR = \frac{I_5}{C_C} \tag{11}$$

where I_5 is the drain current of the transistor M5.

3.1.3. Gain Bandwidth The gain bandwidth GBW is given by:

$$GBW = \frac{g_{m1}}{C_C} \tag{12}$$

3.1.4. Input common mode range

- Positive ICMR V_{Imax}

The maximum input voltage is given by the sum of the voltages from the amplifier input to V_{DD} when the input is at $V_{in}(\max)$.

$$V_{Imax} = V_{DD} - \sqrt{\frac{2I_3}{\mu_0 C_{ox}\frac{W_3}{L_3}}} + V_{th1} \tag{13}$$

where I_3 is the drain current of transistor M3. μ_0 and C_{ox} denote respectively the electron mobility and the oxide capacitance. V_{th1} is the threshold voltage of M1. W_i and L_i denote the gate width and the channel length of the i^{th} transistor.

- Negative ICMR V_{Imin}

The minimum input voltage occurs when the amplifier input is pulled to V_{SS} and M1 and M2 just enter the linear mode.

$$V_{Imin} = V_{SS} + \sqrt{\frac{2I_5}{\mu_0 C_{ox}\frac{W_5}{L_5}}} + V_{th1} \tag{14}$$

3.1.5. Output swing The output swing is obtained from the minimum and maximum output voltages that allowing all transistors to run in the saturation mode.

- Maximum output voltage :

$$V_{Omax} = V_{DD} - \sqrt{\frac{2I_{13}}{\mu_0 C_{ox}\frac{W_{13}}{L_{13}}}} \tag{15}$$

- Minimum output voltage :

$$V_{Omin} = V_{SS} + \sqrt{\frac{2I_{14}}{\mu_0 C_{ox}\frac{W_{14}}{L_{14}}}} \tag{16}$$

The amplifier circuit is designed in CMOS $0.18\mu\mathrm{m}$ technology using Cadence Virtuoso. The design parameters for this amplifier are the transistors channel lengths (L) and widths W, the compensation capacitor C_C and the bias current I_{bias}. During design, the supply voltages $V_{DD(SS)}$ and the load capacity C_L are kept at ± 1.5V and 10pF, respectively. The good operation of the amplifier is ensured by the matching relations of the transistors, M1≡M2, M3≡M4≡M15, M7≡M6, M8≡M9, M5≡M10, M11≡M12 and to reduce the channel modulation effect, the channel lengths are set to three time the minimum value. Table 2 shows the design parameters and their fixed ranges. For simplicity, a small interval for M1 is considered because the current of transistor M5 is twice the current of M1. We also considered a large interval for M13 because the current flowing through it is higher.

We proceed in two different steps, in the first one we optimize only one characteristic keeping fixed the others whereas in the the second step, we gathered the three parameters in a single objective function, giving them the same weight. In all experiments, the other performances are used in constraints to avoid their degradation.

Table 2. Design parameters and ranges.

Variables	Design variables	Low bound	Upper bound
x_1	W_1, W_2 (µm)	1	50
x_2	W_5, W_{10} (µm)	1	100
x_3	W_3, W_4, W_{15} (µm)	1	100
x_4	W_6, W_7 (µm)	1	100
x_5	W_8, W9 (µm)	1	100
x_6	W_{11}, W_{12} (µm)	1	100
x_7	W_{13} (µm)	1	200
x_8	W_{14} (µm)	1	100
x_9	C_c (pF)	3	3
x_{10}	I_{bias} (µA)	45	120

3.2. Problem Formulation

To be successfully designed, amplifiers should be designed according to the specifications required by the application and should meet the design constraints. In all experiments, the WOA is employed to design the circuit taking into account the following constraints, Phase Margin (PM) $\geq 60°$, $V_{Imin} \leq 0.8V$, $V_{Imax} \geq 1.8V$, $V_{Omin} \leq 0.4V$ and $V_{Omax} \geq 1.3V$. In addition, the design specifications for the chosen experiments are given in Table 3.

Table 3. The set of specifications for the LV amplifier

Step 1						Step 2	
experiment 1		experiment 2		experiment 3			
Spec.	Target	Spec.	Target	Spec.	Target	Spec.	Target
A_v	**Maximize**	SR	**Maximize**	GBW	**Maximize**		
SR	$\geq 10V/\mu s$	A_v	$\geq 70dB$	A_v	$\geq 70dB$	f_{total}	**Maximize**
GBW	$\geq 15MHz$	GBW	$\geq 15MHz$	SR	$\geq 10V/\mu s$		

In the second step, the amplifier design is optimized by transforming the optimization problem to a single-objective one by a linear association of the three important functions. We assigned the same weight to the chosen objectives as they are all important for the amplifier design.

The normalized function is given by:

$$f_{\text{total}} = -\alpha \frac{A_v}{A_{\text{vmax}}} - \beta \frac{SR}{SR_{\text{max}}} - \gamma \frac{GBW}{GBW_{\text{max}}} \tag{17}$$

Where $\alpha = \beta = \gamma$ = 1/3, correspond to the weightings parameter for the DC gain, slew rate and gain bandwidth, respectively. These weights can be changed by designers according to each requirement. A_{vmax}, SR_{max} and GBW_{max} are the maximum values of the A_v, the SR and the GBW, respectively.

4. Simulation results and discussion

The amplifier was first optimized using the WOA and by PSO and ACO algorithms for comparison purposes. The algorithms were executed on a computer with an Intel Core i7-7820HQ 10@2.90 GHz (8 CPUs) and 16G memory. Tables 4, 5 and 6 show, respectively, the optimization results and the convergence times for A_v, SR and GBW. These tables also report the simulation results performed by Cadence Virtuoso.

Table 4. DC gain maximization.

algorithms	WOA	PSO	ACO
$A_v(dB)$	**89.22**	88.01	86.53
Convergence time (s)	**1.04**	1.22	5.6
Comparisons of PSO, ACO and WOA in Cadence Virtuoso			
$A_v(dB)$	**88.8**	87.66	85.76

Table 5. Slew rate maximization.

algorithms	WOA	PSO	ACO
$SR(V/\mu s)$	**25.2**	25.10	22.41
Convergence time (s)	**1.06**	1.35	4.78
Comparisons of PSO, ACO and WOA in Cadence Virtuoso			
$SR(V/\mu s)$	**23.92**	23.21	21.05

Table 6. Gain bandwidth maximization.

algorithms	WOA	PSO	ACO
$GBW(dB)$	**25.9**	24.42	21.2
Convergence time (s)	**0.93**	1.21	4.6
Comparisons of PSO, ACO and WOA in Cadence Virtuoso			
$GBW(MHz)$	**24.6**	23.16	19.63

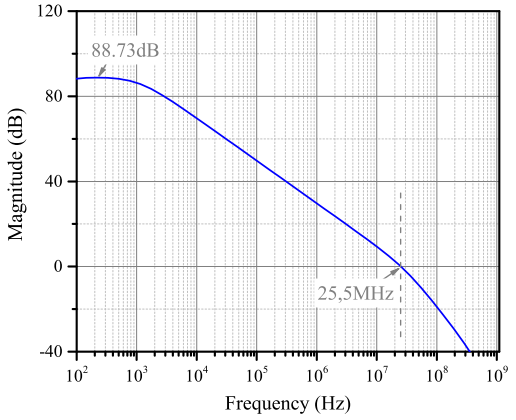
From these tables it can be seen that the proposed algorithm provides the best results compared to the other methods in all experiments. It is evident from the results that all requested specifications are fully satisfied, and reasonably match with the simulation results from CADENCE Virtuoso. It can be also noted that WOA takes a minimum convergence time to attain its global optima.

The results of the multi-objective optimization are presented in table 7. This table also shows the convergence time and the simulation results. We can see that the best trade-offs between the objectives i.e, A_v, SR and GBW, are achieved by the WOA approach in a minimal convergence time. One can also see that the obtained results are in good agreement with the simulations showing that the WOA has a powerful efficiency in analog circuit sizing problems.

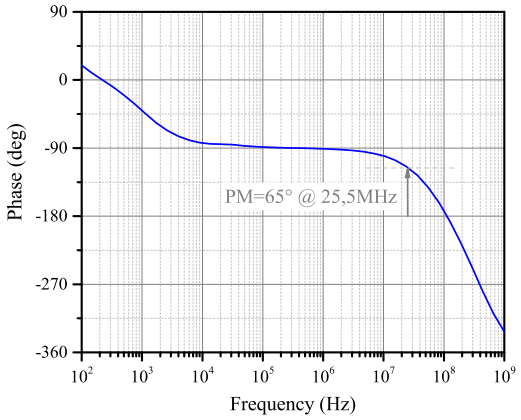
The AC response and the transient simulation of the LV amplifier, as obtained from circuit simulations for typical conditions are shown in Figures. 4 and 5, respectively. The values of the DC gain, the bandwidth gain, the phase margin and the slew rate obtained from the proposed design match reasonably well with those obtained from circuit simulations. This substantiates the validity of the proposed method for the LV amplifier design.

Table 7. DC gain, bandwidth gain and slew rate maximization results.

algorithms	WOA	PSO	ACO
$A_v(dB)$	**89.1**	87.1	87.49
SR(dB)	**19.2**	18.62	16.81
GBW(MHz)	**25.88**	25.7	18.1
Convergence time (s)	**1.12**	1.29	5.4
Comparisons of PSO, ACO and WOA in Cadence Virtuoso			
$A_v(dB)$	**88.73**	87.46	87.69
SR(V/µs)	**20.52**	19.31	16.9
GBW(MHz)	**25.5**	24.46	16.45



(a) The gain versus frequency plot



(b) The phase versus frequency plot

Figure 4. AC Simulation results of the two-stage LV amplifier obtained using the WOA.

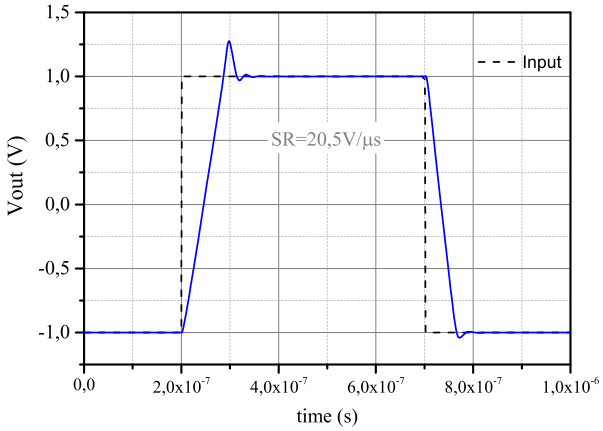
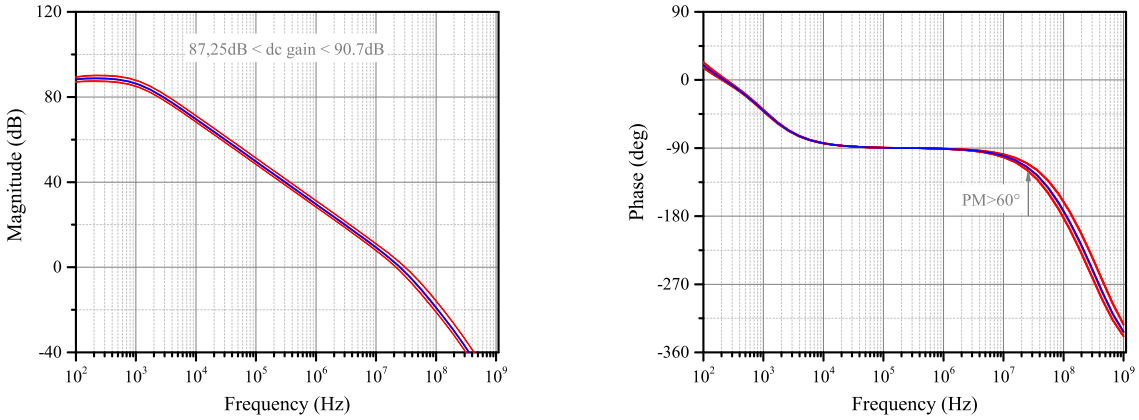


Figure 5. Transient simulations results of LV amplifier.



(a) Magnitude (b) Phase

Figure 6. AC simulations for the LV amplifier, the blue curves refer to typical simulation and the red curves refer to PVT analysis.

Process, voltage and temperature (PVT) variations

To show the robustness of the LV amplifier design, the PVT corners including supply voltage variations ($0.9V_{DD}$, V_{DD}, $1.1V_{DD}$) and temperature changes (-55°C, 27°C , 100°C) are simulated with Cadence for the second step of optimization experiment.

Figure 6 shows the AC simulation results of the PVT analysis. In this figure, the blue curve refers to typical simulation (+27°C, V_{DD}) while the red curves show the simulation results, by varying the temperature and the supply voltages. For typical corners, the open loop gain and the bandwidth are 88.73dB and 25.5MHz and show a maximum variation of 2dB and 3.01MHz which means that the designed circuit has a robust behaviour and is stable against PVT analysis.

The transient simulations to input step of ± 1V are shown in Figure 7 where V_{out} is the output voltage of the amplifier in a negative feedback as a voltage follower. The same temperature and voltage variations are used. For typical corners, the slew rate is $20.5\text{V}/\mu\text{s}$ and shows a maximum variation of $1.5\text{V}/\mu\text{s}$.

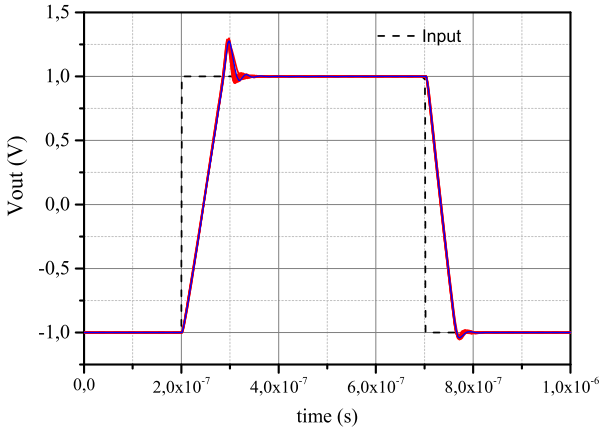


Figure 7. Transient simulations for the LV amplifier, the blue curves refer to typical simulation and the red curves refer to PVT analysis.

5. Conclusion

In this paper, a new optimization method for analog circuit design is successfully introduced. It is inspired by the whale strategy for food searching. The test circuit is the two-stage low voltage amplifier. For comparison purposes, the ACO and PSO algorithms are used for the same problem resolution. Before their application, some robustness tests have been carried out to verify the correct convergence of these used algorithms. Through many experiments, we have shown that this algorithm allows to achieve rapidly better results despite the great complexity of the optimized circuit. The achieved results show that the proposed algorithm beside providing efficient results, can be useful for the optimization of analog circuits. The optimization results are in good agreement with obtained simulations with the Cadence Virtuoso in CMOS 0.18µm technology.

REFERENCES

1. "Wsts home n.d. https://www.wsts.org/(accessed february 25, 2021)."
2. G. G. Gielen and R. A. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proceedings of the IEEE*, vol. 88, no. 12, pp. 1825–1854, 2000.
3. E. Yilmaz and G. Dundar, "Analog layout generator for cmos circuits," *IEEE Transactions on computer-aided design of integrated circuits and systems*, vol. 28, no. 1, pp. 32–45, 2008.
4. R. S. Zebulum, M. A. Pacheco, and M. M. B. Vellasco, *Evolutionary electronics: automatic design of electronic circuits and systems by genetic algorithms*. CRC press, 2018.
5. A. Lberni, A. Sallem, M. A. Marktani, N. Masmoudi, A. Ahaitouf, and A. Ahaitouf, "Influence of the operating regimes of mos transistors on the sizing and optimization of cmos analog integrated circuits," *AEU - International Journal of Electronics and Communications*, p. 154023, 2021.
6. A. Lberni, A. Sallem, M. A. Marktani, A. Ahaitouf, N. Masmoudi, and A. Ahaitouf, "An efficient multi-objective simulation-based approach for low voltage low power analog ics," in *2020 IEEE International Conference on Design Test of Integrated Micro Nano-Systems (DTS)*, 2020, pp. 1–5.
7. A. Sallem, P. Pereira, M. Fakhfakh, and H. Fino, "A multi-objective simulation based tool: application to the design of high performance lc-vcos," in *Doctoral Conference on Computing, Electrical and Industrial Systems*. Springer, 2013, pp. 459–468.
8. E. Afacan, "Inversion coefficient optimization based analog/rf circuit design automation," *Microelectronics Journal*, vol. 83, pp. 86–93, 2019.
9. A. Patanè, A. Santoro, P. Conca, G. Carapezza, A. La Magna, V. Romano, and G. Nicosia, "Multi-objective optimization and analysis for the design space exploration of analog circuits and solar cells," *Engineering Applications of Artificial Intelligence*, vol. 62, pp. 373–383, 2017.
10. R. Martins, N. Lourenço, and N. Horta, "Multi-objective optimization of analog integrated circuit placement hierarchy in absolute coordinates," *Expert Systems with Applications*, vol. 42, no. 23, pp. 9137–9151, 2015.
11. A. Lberni, A. Sallem, M. A. Marktani, A. Ahaitouf, N. Masmoudi, and A. Ahaitouf, "Simulation-based optimization for automated design of analog/rf circuits," in *WITS 2020*. Springer, 2022, pp. 389–399.

12. A. Lberni, M. A. Marktani, A. Ahaitouf, and A. Ahaitouf, "Efficient butterfly inspired optimization algorithm for analog circuits design," *Microelectronics Journal*, vol. 113, p. 105078, 2021.
13. A. Lberni, A. Ahaitouf, M. A. Marktani, and A. Ahaitouf, "Sizing of second generation current conveyor using evolutionary algorithms," in *2019 International Conference on Intelligent Systems and Advanced Computing Sciences (ISACS)*. IEEE, 2019, pp. 1–5.
14. B. Benhala and A. Ahaitouf, "Ga and aco in hybrid approach for analog circuit performance optimization," in *2014 International Conference on Multimedia Computing and Systems (ICMCS)*. IEEE, 2014, pp. 1590–1595.
15. A. Lberni, M. A. Marktani, A. Ahaitouf, and A. Ahaitouf, "Adaptation of the whale optimization algorithm to the optimal sizing of analog integrated circuit: Low voltage amplifier performances," in *2020 IEEE 2nd International Conference on Electronics, Control, Optimization and Computer Science (ICECOCS)*, 2020, pp. 1–6.
16. A. Sallem, B. Benhala, M. Kotti, M. Fakhfakh, A. Ahaitouf, and M. Loulou, "Simulation-based multi-objective optimization of current conveyors: Performance evaluations," in *7th International Conference on Design & Technology of Integrated Systems in Nanoscale Era*. IEEE, 2012, pp. 1–5.
17. M. N. Sabry, I. Nashaat, and H. Omran, "Automated design and optimization flow for fully-differential switched capacitor amplifiers using recycling folded cascode ota," *Microelectronics Journal*, p. 104814, 2020.
18. A. Lberni, M. Alami Marktani, A. Ahaitouf, and A. Ahaitouf, "Application of hpsgwo to the optimal sizing of analog active filter," in *Proceedings of the 2nd International Conference on Electronic Engineering and Renewable Energy Systems*, B. Hajji, A. Mellit, G. Marco Tina, A. Rabhi, J. Launay, and S. E. Naimi, Eds. Singapore: Springer Singapore, 2021, pp. 309–315.
19. S. Mirjalili and A. Lewis, "The whale optimization algorithm," *Advances in engineering software*, vol. 95, pp. 51–67, 2016.
20. M. Fakhfakh, Y. Cooren, A. Sallem, M. Loulou, and P. Siarry, "Analog circuit design optimization through the particle swarm optimization technique," *Analog integrated circuits and signal processing*, vol. 63, no. 1, pp. 71–82, 2010.
21. B. Benhala, M. Kotti, A. Ahaitouf, and M. Fakhfakh, "Backtracking aco for rf-circuit design optimization," in *Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*. IGI Global, 2015, pp. 158–179.
22. P. Dutta and A. Kumar, "Modelling of liquid flow control system using optimized genetic algorithm," *Statistics, Optimization & Information Computing*, vol. 8, no. 2, pp. 565–582, 2020.
23. P. Pereira, M. Kotti, H. Fino, and M. Fakhfakh, "Metaheuristic algorithms comparison for the lc-voltage controlled oscillators optimal design," in *2013 5th International Conference on Modeling, Simulation and Applied Optimization (ICMSAO)*. IEEE, 2013, pp. 1–6.
24. N. Sayyadi Shahraki and S. H. Zahiri, "Multi-objective learning automata for design and optimization a two-stage cmos operational amplifier," *Iranian Journal of Electrical and Electronic Engineering*, vol. 16, no. 2, pp. 201–214, 2020.
25. P. E. Allen and D. R. Holberg, *CMOS analog circuit design*. Elsevier, 2011.